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P599 - USM™ Main PMC

- **Main PMC for USM™ Universal Submodules**
- **1 USM™ slot**
- **1 FPGA 33,216 LE (for user-defined I/O and Nios® soft core)**
- **32 MB DDR2 SDRAM**
- **2 MB Flash**
- **-40 to +85°C with qualified components**

USM™ Universal Submodules make PMC modules more flexible than ever. The main PMC P599 gets its specific function through the IP cores implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM™ which is simply plugged on the P599.
The same USM™ may also be used on XMCs, conduction-cooled PMCs or M-Module™ main modules. A new design is then limited to the USM™ module and the FPGA content and therefore saves development time and costs. A Nios® soft processor implemented in the Cyclone® II FPGA by Altera® provides local intelligence where needed. The I/O signals are led to the USM™ and then to a SCSI connector at the front of the P599.

The growing range of Wishbone-based standard IP cores from MEN comprise different UARTs, Ethernet, fieldbus interfaces, graphics, digital I/O etc. For users who like to write and/or implement specific IP cores on their own a complete FPGA USM™ development kit is available.
The USM™ concept has been developed for harsh environments. Therefore, the P599 uses robust connectors to the USM™, while all other components are soldered, and operates in a -40 to +85 °C temperature range with qualified components.
The P599 is a PMC mezzanine card suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate PMC carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

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Technical Data

Functionality
- User-defined through FPGA
- Line drivers and/or additional hardware implemented on USM™ Universal Submodule (not included)

Memory
- 32MB SDRAM memory
  - Soldered
  - DDR2
  - 132MHz memory bus frequency
  - FPGA-controlled
- 2MB non-volatile Flash
  - For FPGA data and Nios® firmware
  - FPGA-controlled

FPGA
- Standard factory FPGA configuration:
  - Main bus interface
  - Altera® SOPC Unit incl. Nios® II/f soft processor, GPIO, UART and DDR2 SDRAM control
  - Wishbone-to-Avalon®/Avalon®-to-Wishbone bridges
  - Chameleon Table V2
  - Interrupt controller, SMBus controller
  - PCI to Wishbone bridge, ID EEPROM emulation
  - 16Z045_FLASH - Flash interface
  - 16Z034_GPIO - GPIO controllers (2 IP cores, for onboard LEDs and 8-bit I/O)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

USM™ Slot
- One slot for a standard USM™ module
- For implementation of line drivers and/or additional hardware

Miscellaneous
- Eight front-panel LEDs, FPGA-controlled
- I²C interface to detect the USM™ module

PMC Characteristics (PCI)
- Compliant with PCI Specification 2.2
- 32-bit/33-MHz, 3.3V V(I/O)
- Target

Peripheral Connections
- Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector

Electrical Specifications
- Isolation voltage:
  - Voltage depends on implementation and signal routing of USM™
- Supply voltage/power consumption:
  - +5V (-3%/+5%), FPGA idle / US0 plugged: 83mA, memory test / US0 plugged: 109mA
  - +3.3V (-5%/+5%), FPGA idle / US0 plugged: 74mA, memory test / US0 plugged: 82mA
- MTBF: 669,963h @ 40°C according to IEC/TR 62380 (RDF 2000)

Mechanical Specifications
- Dimensions: conforming to IEEE 1386.1
- Weight: 65g (w/o USM™ module)

Environmental Specifications
- Temperature range (operation):
  - -40..+85°C (qualified components)
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support
- Nios® sample design for Quartus® II development tools
- Flash update tools for Windows®, Linux, VxWorks®
- Driver software depending on implemented FPGA functions
- For more information on supported operating system versions and drivers see Software.

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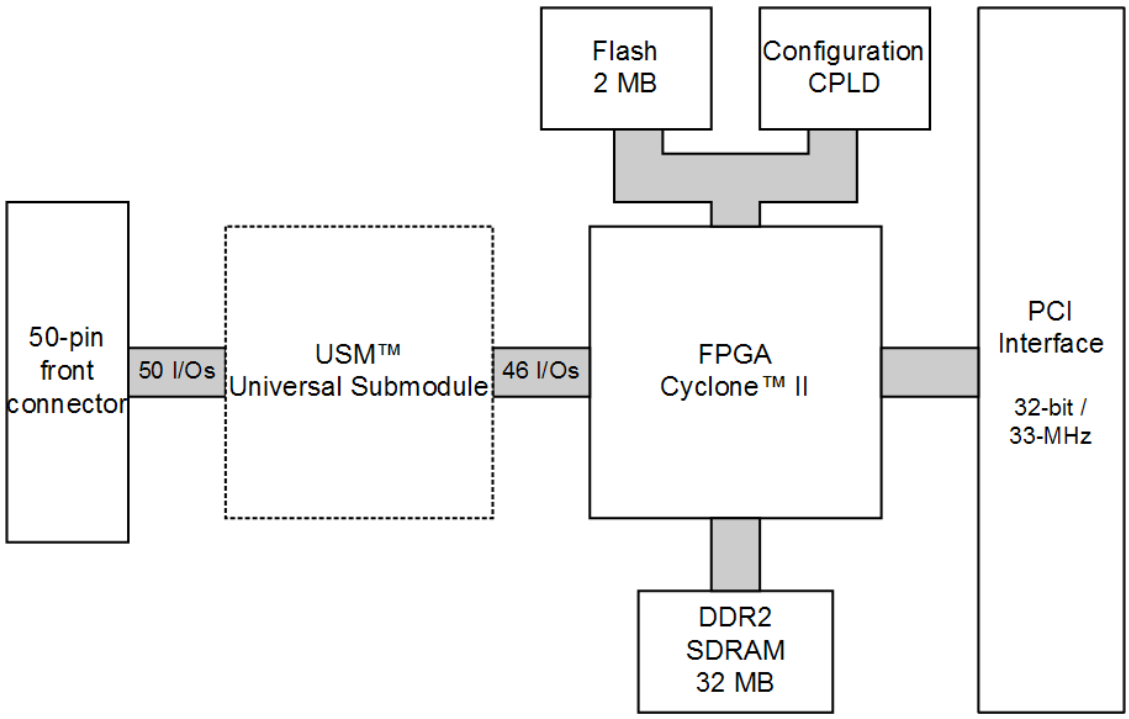
Diagram



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FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® II EP2C35
  - 33,216 logic elements
  - 483,840 total RAM bits
  - Supports Nios® II soft processor
- Connection
  - Functions can be linked to Wishbone or Avalon® bus
  - Available pin count: 46 pins (FPGA to USM™)
  - Functions available via USM™ at front I/O connector
- MEN offers an FPGA Development Package as well as Flash update tools for different operating systems.

MEN IP Cores

- MEN offers a large number of standard IP cores.
- Examples:
  - IDE (e.g. PIO mode 0, UDMA mode 5)
  - UARTs
  - CAN bus
  - Display control
  - Fast Ethernet (10/100Base-T)
  - ...
- For IP cores developed by MEN please refer to our IP core overview.
  - IP Core compare chart (PDF)
- MEN also offers development of new (customized) IP cores.

Third-Party IP Cores

- Third-party IP cores can also be used in combination with MEN IP cores.
- Examples:
  - www.altera.com
  - www.opencores.org

FPGA Design Environment

- Altera® offers free download of Quartus® II Web Edition
  - Complete environment for FPGA and CPLD design
  - Includes schematic- and text-based design entry
  - Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
  - SOPC Builder system generation software
  - Place-and-route, verification, and programming
- Altera® Quartus® II Web Edition FPGA design tool

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Ordering Information

Standard Hardware

15P599-00 USM main PMC, -40..85°C with qualified components

Related Hardware

19P599-00 PMC USM FPGA development kit consisting of 1 FPGA-based universal PMC P599, 1 bare USM Universal Submodule US0, 1 eval board AD99 for USM/FPGA development, 1 SA-Adapter SA1 (RS232), connection cable, FPGA/Nios example project including PCI core (key download), 0..+60°C

Miscellaneous

05P599-00 PMC/M-Module cable, 2m, with 50-pin HP D-Sub 50 M both sides, 0..+60°C

08US00-00 Universal Submodule for prototyping, -40..+85°C qualified

FPGA Packages

16P599-00 Nios PMC USM FPGA Development Package (MEN) (without Altera Quartus II) (license included in PMC USM FPGA Development Kit)

Software: OS independent

13Z017-06 MDIS4/2004 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

13Z100-91 Linux FPGA update tool (MEN)

Software: Windows

13Z017-70 MDIS4/2004 Windows driver (MEN) for 16Z034_GPIO devices

13Z100-70 Windows FPGA update tool (MEN)

Software: VxWorks

13Z100-60 VxWorks FPGA update tool (MEN)

Software: FPGA

16P599-00 Nios PMC USM FPGA Development Package (MEN) (without Altera Quartus II) (license included in PMC USM FPGA Development Kit)

Documentation

20P599-00 P599 User Manual

20US00-00 USM Specification

21M199-00 P599/M199 Programmer's Guide

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the P599 online data sheet under » www.men.de.

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