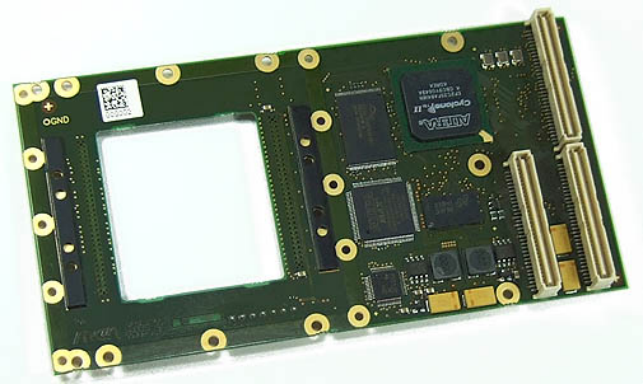
P598 – Conduction-Cooled FPGA-based USM Main PMC

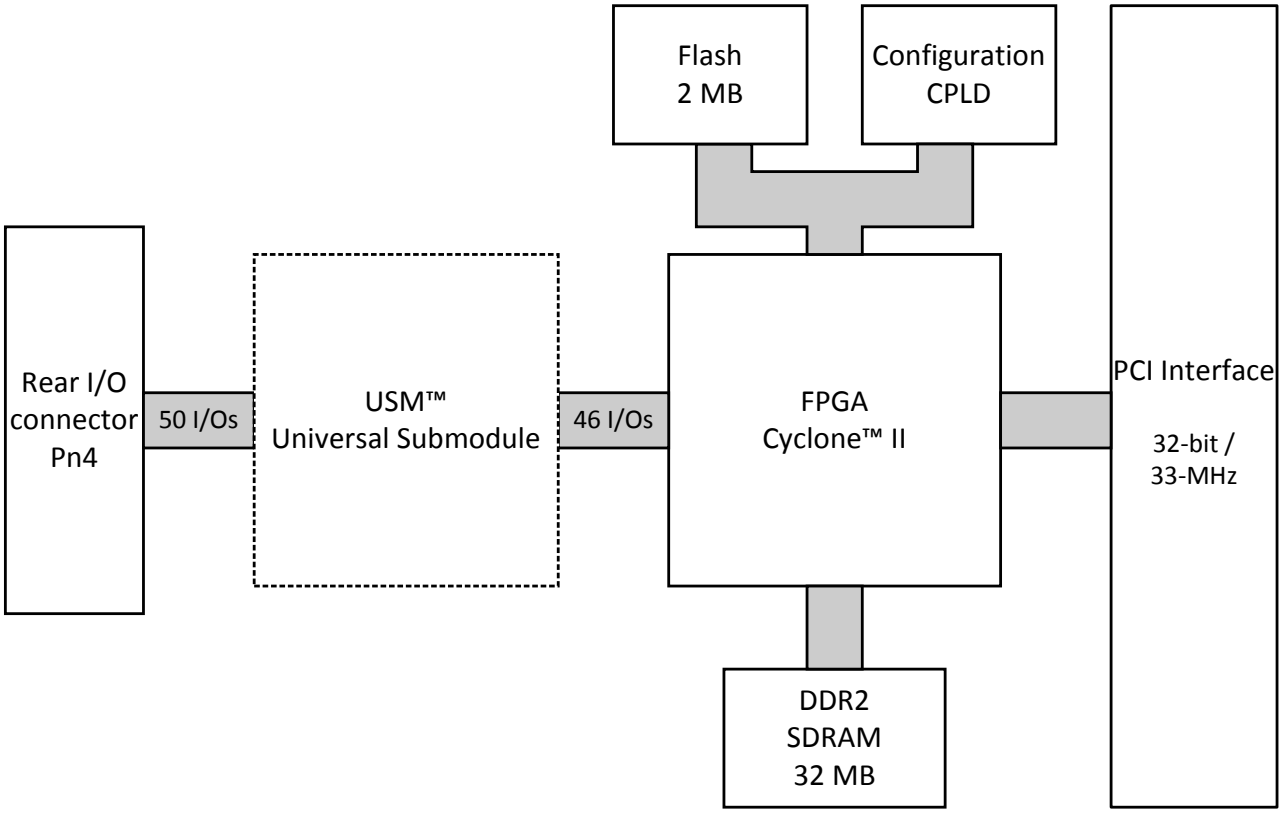
- **Main PMC for USM Universal Submodules**
- **Conduction-cooled (CCPMC)**
- **1 USM slot**
- **1 FPGA 33,216 LE (for user-defined I/O and Nios® soft core)**
- **32 MB DDR2 SDRAM**
- **2 MB Flash**
- **-40 to +85°C with qualified components**



USM Universal Submodules make PMC modules more flexible than ever. The conduction-cooled main PMC P598 gets its specific function through the IP cores implemented inside the onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM which is simply plugged on the P598.
The same USM may also be used on convection-cooled PMCs and XMCs or main M-Modules. A new design is then limited to the USM module and the FPGA content and therefore saves development time and costs. A Nios® soft processor implemented in the Cyclone® II FPGA by Altera® provides local intelligence where needed.

The growing range of Wishbone-based standard IP cores from MEN comprise different UARTs, Ethernet, fieldbus interfaces, digital I/O etc. For users that like to write and/or implement specific IP cores on their own a complete development kit is available. The kit is based on a function-identical convection-cooled PMC module with front I/O.
The USM concept has been developed for harsh environment. Therefore, the P598 uses robust connectors to the USM, while all other components are soldered, and operates in a -40 to +85 °C temperature range with qualified components.
The P598 is a conduction-cooled PMC mezzanine card suitable for any compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

Diagram


Flash
2 MB
Configuration
CPLD
Rear I/O
connector
Pn4
50 I/Os
USM™
Universal Submodule
46 I/Os
FPGA
Cyclone™ II
PCI Interface
32-bit /
33-MHz
DDR2
SDRAM
32 MB

Technical Data

Functionality	■ User-defined through FPGA ■ Line drivers and/or additional hardware implemented on USM Universal Submodule (not included)
Memory	■ 32MB SDRAM memory □ Soldered □ DDR2 □ 132MHz memory bus frequency □ FPGA-controlled ■ 2MB non-volatile Flash □ For FPGA data and Nios® firmware □ FPGA-controlled
FPGA	■ Standard factory FPGA configuration: □ Main bus interface □ Altera® SOPC Unit incl. Nios® II/f soft processor, GPIO, UART and DDR2 SDRAM control □ Wishbone-to-Avalon®/Avalon®-to-Wishbone bridges □ Chameleon Table V2 □ Interrupt controller, SMBus controller □ PCI to Wishbone bridge, ID EEPROM emulation □ 16Z045_FLASH - Flash interface □ 16Z034_GPIO - GPIO controllers (2 IP cores, for onboard LEDs and 8-bit I/O) ■ The FPGA offers the possibility to add customized I/O functionality. See FPGA.
USM Slot	■ One slot for a standard USM module ■ For implementation of line drivers and/or additional hardware
Miscellaneous	■ Eight onboard LEDs, FPGA-controlled ■ I²C interface to detect the USM module
PMC Characteristics (PCI)	■ Compliant with PCI Specification 2.2 ■ 32-bit/33-MHz, 3.3V V(I/O) ■ Target
Peripheral Connections	■ Via Pn4 rear I/O connector
Electrical Specifications	■ Isolation voltage: □ Voltage depends on implementation and signal routing of USM ■ Supply voltage/power consumption: □ +5V (-3%/+5%), FPGA idle / US0 plugged: approx. 118mA, memory test / US0 plugged: 122mA □ +3.3V (-5%/+5%), FPGA idle / US0 plugged: 76mA, memory test / US0 plugged: 82mA ■ MTBF: 848,597h @ 40°C according to IEC/TR 62380 (RDF 2000)
Mechanical Specifications	■ Dimensions: conforming to IEEE 1386.1 ■ In accordance with VITA 20 (proposed Draft Standard for Conduction Cooled PMC) ■ Weight: 36g (w/o USM module)
Environmental Specifications	■ Temperature range (operation): □ -40..+85°C (qualified components), conduction-cooled □ Airflow: min. 10m³/h ■ Temperature range (storage): -40..+85°C ■ Relative humidity (operation): max. 95% non-condensing ■ Relative humidity (storage): max. 95% non-condensing ■ Altitude: -300m to + 3,000m ■ Shock: 15g/11ms ■ Bump: 10g/16ms ■ Vibration (sinusoidal): 2g/10..150Hz ■ Conformal coating on request
Safety	■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

Technical Data

EMC	■ Radio disturbance: no connection outside housing, therefore radio disturbance not relevant ■ ESD/burst: no external interface connector, therefore ESD and burst not relevant
Software Support	■ Flash update tools for Linux, Windows®, VxWorks®, QNX® ■ Driver software depending on implemented FPGA functions ■ For more information on supported operating system versions and drivers see Downloads.

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration	■ Customized I/O functions can be added to the FPGA. ■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility. ■ You can find more information on our web page "User I/O in FPGA"
FPGA Capabilities	■ FPGA Altera® Cyclone® II EP2C35 □ 33,216 logic elements □ 483,840 total RAM bits □ Supports Nios® II soft processor ■ Connection □ Functions can be linked to Wishbone or Avalon® bus □ Available pin count: 46 pins (FPGA to USM) □ Functions available via USM at rear I/O connector ■ MEN offers an FPGA Development Package as well as Flash update tools for different operating systems. □ Package comes with function-identical convection-cooled PMC module with front I/O □ Only for development of FPGA, independent of conduction cooling
MEN IP Cores	■ MEN offers a large number of standard IP cores. ■ Examples: □ IDE (e.g. PIO mode 0, UDMA mode 5) □ UARTs □ CAN bus □ Display control □ Fast Ethernet (10/100Base-T) □ ... ■ For IP cores developed by MEN please refer to our IP core overview. □ IP Core compare chart (PDF) ■ MEN also offers development of new (customized) IP cores.
Third-Party IP Cores	■ Third-party IP cores can also be used in combination with MEN IP cores. ■ Examples: □ www.altera.com □ www.opencores.org
FPGA Design Environment	■ Altera® offers free download of Quartus® II Web Edition □ Complete environment for FPGA and CPLD design □ Includes schematic- and text-based design entry □ Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software □ SOPC Builder system generation software □ Place-and-route, verification, and programming ■ Altera® Quartus® II Web Edition FPGA design tool

Ordering Information

Standard P598 Models	**15P598-00**	USM main PMC, conduction cooled, -40..+85°C with qualified components
Miscellaneous Accessories	**05P000-01**	25 mounting screw sets to fix PMC/XMC modules on carrier boards
	08US00-00	Universal Submodule for prototyping, -40..+85°C qualified
Software: FPGA	**16P599-00**	Nios® PMC USM FPGA Development Package (MEN) (without Altera® Quartus® II) (license included in PMC USM FPGA Development Kit)
Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO
	13Z100-91	Linux FPGA update tool (MEN)
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	13P599-77	Windows® Installset (MEN) for P599, P598 and PMC USM FPGA development kit (Includes all free drivers developed by MEN for the supported hardware.)
	13Y018-70	Windows® 64-bit FPGA update tool (MEN)
Software: VxWorks®	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO
	13Z100-60	VxWorks® FPGA update tool (MEN)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO
	13Z100-40	QNX® FPGA update tool (MEN)

For operating systems not mentioned here contact MEN sales.

Documentation	Compare Chart mezzanine functions on PMC/XMC and PC-MIP® » Download	
	20P598-00	P598 User Manual
	20US00-00	USM Specification
	21M199-00	P599/M199 Programmer's Guide

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