IC-INT-VPX6a

Dual Intel® Core™ i7 Gen2 SBC

With greater power, flexibility, functions and efficiency, the **IC-INT-VPX6a** is a concentrate of IC's experience in high computing solutions for VPX systems.

Its two Intel® Core™ i7 Gen 2 processors offer unmatched technology and performance, taking advantage of all last Intel® improvementss : Advanced Vector Extensions™ (AVX), Hyper-Threading Technology, HD Graphics 3000 with 3D &OpenGL, Turbo Boost 2.0 at up to 3.2 GHz...

Beyond the computing power of these two processors, with one FPGA Kintex-7, two inter-domain PCI Express switches and a GigaEthernet switch, the IC-INT-VPX6a provides all the functionality of an on-board system.

The **IC-INT-VPX6a** is delivered with the IC Boot Loader which allows optimized power-up sequences. Our Fabric Management Software (**Multiware**) provides efficient data transfers and events management between PCIe domains over non transparent bridges (NTB).

Description

Intel® Core™ i7 computing nodes (A & B) are populated with Dual Core Sandy Bridge processors associated with QM67 chipsets.

The **IC-INT-VPX6a** provides versatile PCIe backplane configurations thanks to two PCIe switches, each attached to both CPUs via x8 links; The first switch provides 16 lanes (***2 x8*** or ***1 x8 / 2 x4*** or ***4 x4***) on P1, while the second provides 8 lanes (***1 x8 / 2 x4***) on P2, 4 lanes to the FPGA (***1 x4***) and 4 lanes to the XMC slot.
Each chipset is also directly connected to P2 via a PCIe ***x4*** link.

The XMC site (PCIe ***x4*** link) provides 20 differential I/O pairs routed from Pn6 to P6 in accordance with X12d+X8d pattern of VITA 46.9.

The **IC-INT-VPX6a** implements an ultra low latency GE switch attached to each CPU and offering five GigE ports. One rear GigaEthernet port is connected directly to each processor (please contact us for other available options).

The **IC-INT-VPX6a** also takes advantage of the media capabilities of the Intel chipsets to provide two HDMI interfaces, GPIOs, two USB and one SATA port per processor.
For storage, the board features soldered SATA NAND SSD.

Finally, the **IC-INT-VPX6a** implements an FPGA interfaced with one PCIe switch (***x4***), dedicated to customer applications. The selected Kintex-7 FPGA deliver high signal processing performance, low power consumption and the serial bandwidth claimed by the most demanding embedded applications.

The FPGA is connected directly to the P3/P4 connectors (SERDES/GPIOs) and an optional FMC site, fully compliant with the FPGA Mezzanine Card standard (VITA 57.1). Coupled with optional IPs, the FPGA allows to expand the communication capabilities of the board. For example, it is possible to implement up to four * **10 Gigabit Ethernet ports** (XAUI or 10GBase-KR).

The FMC and the board can also use to Pn6 connector to route additional differential pairs (100 Ohms) from the FMC module directly to the VPX backplane (P6).

The **IC-INT-VPX6a** is compliant at a minimum with the following *OpenVPX* profiles (VITA 65): SLT6-PAY-4F2T, SLT6-PAY-8F, SLT6-PAY-2F2U2T.

Main features

Processor Unit (per processor)
- ▸ Intel® Core™ i7 2655LE
  - • Core speed = 2.2GHz
  - • Cache = 6MB
  - • Thermal design power = 25W
- ▸ DDR3-1333 with ECC
- ▸ boot flash memory
- ▸ on board SATA SSD

Communication subsystem (per processor)
- ▸ 2 * PCIe x8 (1 per PCIe switch)
- ▸ 2 * USB 2.0 ports (1 front / 2 rear)
- ▸ 1 * Console port (rear)
- ▸ 1 * rear SATA interfaces
- ▸ 2 * HDMI interfaces (1 front / 1 rear)
- ▸ GPIOs (Rear)
- ▸ 1 * GigE port (attached to the switch)
- ▸ 1 * 1000Base-BX or 10/100/1000BaseT port (factory setting / rear)

Ethernet Switch
- ▸ 5 * GigE ports (rear: 2 * 1000Base-T / 2 * 1000Base-BX, front:: 1 * 1000Base-T)

Extension (node A)
- ▸ 1 * XMC slot (PCIe x4 on Pn5)
- ▸ 20 differential pairs (from Pn6 to P6 - X12d+X8d)

FPGA
- ▸ 1 * Kintex-7 (XC7 KX70 / *KX160 on demand*)

optional FMC site (exclusive with the XMC site):
- ▸ 80 LVDS (from FPGA)
- ▸ GTX x4 (from FPGA)
- ▸ 16 differential pairs (to P5, option)

Miscellaneous
- ▸ Status LEDs
- ▸ PIC µ-controller for System Management (per VITA 46.11)
- ▸ Power supply monitoring / Temperature sensor...
- ▸ Engineering kit for debug : JTAG/COP...
- ▸ 6U Rear Transition Module

The **IC-INT-VPX6a** is a 6U x 4HP (1") VPX board compliant with 6U module definitions of the VITA 46.0 standard (0.80 or 0.85" : please consult us).
It is available in air-cooled and conduction cooled (without front I/O) versions compliant with VITA 47 classes.

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On-board firmware

Interface Concept Single Board Computers based on Intel CPUs use the new UEFI firrmware technology.
This Boot Loader, **developed and tested by our R&D team**, implements all the initializations and optimized PBITs while ensuring the shortest boot time before launching the UEFI shell or loading the Operating System from storage devices (CD, DVD, HDD, USB…) or network.

When the final application is running, Runtime services remain in memory thus allowing the user to access UEFI variables for monitoring (e.g. PBIT results) or setup operations.
On request, we can customize the Boot Loader to keep only what is strictly necessary for customer's applications.

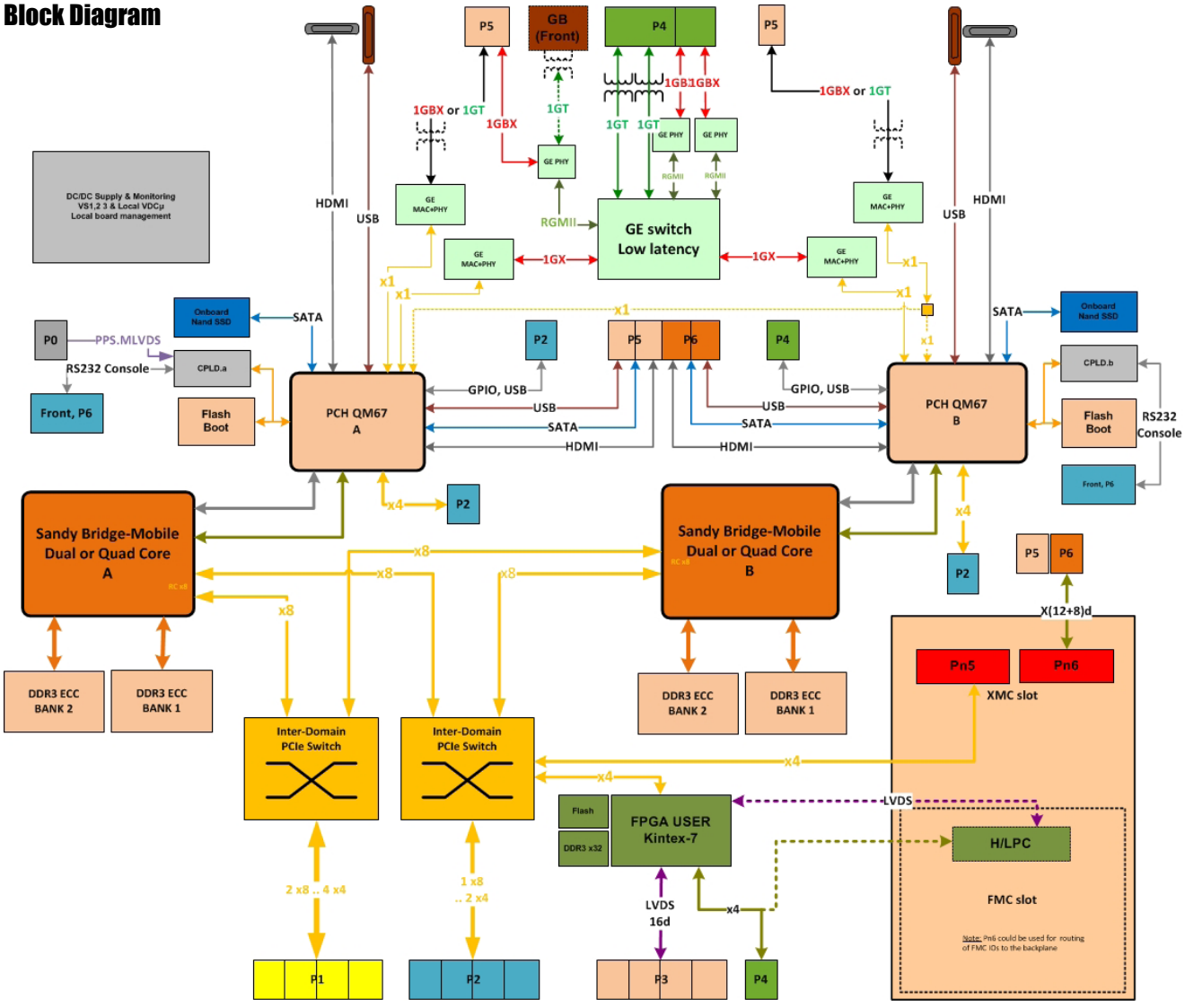
OS support

Interface Concept provides LSP Linux® distributions (IC SDK, others...) and VxWorks® 6.9.

Multiware

In oder to empower customers to concentrate their efforts on their most critical tasks, Interface Concept developed a Fabric Management Software implementing optimized services between PCIe domains over non transparent bridges NTB) such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc.
(please consult us for details)

Block Diagram



Environmental Specifications:

Please consult the **IC-INT-VPX6a** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 573 030** - email : **info@interfaceconcept.com**

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

INTERFACE CONCEPT
Corporate Headquarters • 29000 Quimper • FRANCE • TEL +33 (0)2 98 573 030 • FAX +33 (0)2 98 573 000
info@interfaceconcept.com