TIC-PPC-VPX3a

3U VPX MPC8640D Single Board Computer

ELMA
Your Solution Partner

The TIC-PPC-VPX3a is powered by a a single MPC8640D processor to deliver best in class performance with an AltiVec 128 bit vector processing engine.

Designed for applications requiring a very high level of performance in a compact 3U form factor, the TIC-PPC-VPX3a board provides a very flexible combination of interfaces, supporting OpenVPX's high bandwidth serial switched fabrics such as PCI Express and Serial RapidIO.

The TIC-PPC-VPX3a, paired with our TIC-FEP-VPX3b front end processor and our TIC-XMC-VPX3a Carrier for XMCs, is the ideal solution to build high computing platforms, FPGA processing configurations or embedded computers.

Description

The MPC8640D processor in the TIC-PPC-VPX3a uses e600 cores and high-speed interconnect technology to balance processor performance with I/O system throughput. Each core is a high performance, superscalar design supporting multiple execution units. Each includes 32-Kbyte separate I/D L1 cache and a 1-Mbyte L2 cache.

TIC-PPC-VPX3a supports up to 4GB of DDR2-ECC. The integration of the system controller provides superior memory bandwidth and memory latency performance.

The OpenVPX standard allows system designers to have flexibility in topology for large mesh designs, or designs passing heavy traffic on particular backplane segments. A PCI Express switch allows versatile coupling between the processor and the other slots. The P1A and P1B x4 links can be aggregated to form a PCIe x8 link or spread to form four PCIe x2 links. In addition, the P1C link can be either a PCI-Express x4 link or a Serial-RapidIO x4 link. These configurations are hardware selectable by the user.

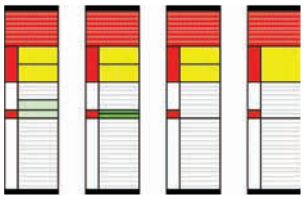
The TIC-PPC-VPX3a board also provides four Gigabit Ethernet ports.

A Samtec QSE connector, enables adding an optional IO Mezzanine interfaced with the processor via a PCIe x1, x2 or x4 link and with the VPX P2 connector via 16 differential pairs. Powered by 5V and 3.3V, this mezzanine allows customization of the IOs capabilities of the TIC-PPC-VPX3a.

OpenVPX

The TIC-PPC-VPX3a is compliant with the following OpenVPX profiles (VITA 65) :

- MOD3-PAY-2F2U-16.2.3-2
- MOD3-PAY-2F2T-16.2.5-2
- MOD3-PAY-1D-16.2.6-1
- MOD3-PAY-2F-16.2.7-1



Main Features

Processor Unit

- 1 MPC8640 Dual-Core running at 1 GHz with :
  - L1 cache : 32KB Inst. and 32KB Data
  - 1MB of L2 integrated cache with parity
- 2 DDRII banks (up to 2 GBytes each) with ECC
- Mirror-Bit Flash (up to 512 MBytes)
- 512 KB of nvSRAM (non-volatile memory)
- 1 Calendar clock with supercap backup
- 1 Elapsed Time Counter
- 1 thermal monitoring sensor
- 1 power supply monitoring sensor
- 1GB of Soldered NAND flash (up to 8GB/SLC or 16GB/MLC)

Communication subsystem

- 8 lanes available as one PCIe x8 or two PCIe x4 or four PCIe x2 links (hardware setting)
- 4 lanes available as one PCIe x4 or one SRIO x4 link (hardware setting)
- PIC µ-controller for System Management (per VITA 46.11)
- 16* differential pairs (optional)
- 1* RS422 UART available on P2 2 Gigabit Ethernet ports available either as two 1000BT interfaces or two 1000KX (or SGMII) interfaces on P1 (factory setting)
- 2 Gigabit Ethernet ports available either as 2*1000BT interfaces on front RJ45 connectors or as 2*1000KX (or SGMII) interfaces on P2
- 2 Gigabit Ethernet ports available either as two 1000BT interfaces or two 1000KX (or SGMII) interfaces on P1 (factory setting)
- RS232 UART available on a front mini USB connector and P1
- Eight GPIOs on P2 (3.3V LVTTL Level)
- I2C bus for Management interface
- Status LEDs

Accessories

- Engineering kit for debug : JTAG/COP, console,...
- 3U Rear Transition Module

TIC-PPC-VPX3a is available in standard, extended, rugged and conduction-cooled grades.

ACT/Technico™ brand of Embedded Computing Products


SBCs

I/O


Software

Design & Documentation

Chassis


Ethernet Switches

TIC-PPC-VPX3a

On-board firmware

Our basic firmware manages Freescale's new MPC8641D and its internal chipset initialization. This on-board firmware, UBOOT, is an efficient set of software stored in secure flash.

UBoot

UBoot is called by the reset vector when the board is powered up. It initializes the PowerPC and its system controller, and performs a comprehensive Power-on self-tests (PBIT), before jumping into different applications according to the values stored in memory. The firmware allows loading files from Ethernet via Bootp, running files in RAM or flashing them. In addition, it allows monitoring functions such as display or modification of the RAM data. UBoot also enables the user to perform maintenance tests.

Software

IC_Bios

This module allows the user to access the specific TIC-De6-VMEa hardware resources via an easy-to-use API. This module is used as a library with Vx-Works.

IC-BSP basic

These Board Support Packages (BSPs) are based on the standard distribution of the Operating System. They handle hardware initialization, interrupt handling and generation, hardware clock and timer services, memory management, PCI management, mapping of memory spaces, serial ports, GE MAC driver ports, USB2 driver, SATA drivers with RAID functions (Linux only), NAND and NOR Flash files systems, etc.

BSPs are available for VxWorks® 6.6 (or latest) and LSP for Linux® operating systems. Other RTOS (LynxOS, Integrity, etc.) can be ported on request. Vxworks-SMP and Linux-SMP are supported on dual core configurations.

Interface features

Front connectors

- 2*Giga Ethernet port (1000BT - RJ45) (also available on P2)
- 1*RS232 UART (also available on P1)
- LEDs

P1 connector

- 8 lanes available as one PCIe x8 or two PCIe x4 or four PCIe x2 links (hardware setting)
- 2 Gigabit Ethernet ports available either as 2*1000BT interfaces or 2*1000KX (or SGMII) interfaces (factory setting)
- 1*RS232 UART

P2 connector

- One RS422 UART
- Two Gigabit Ethernet ports available as 1000KX (or SGMII) interfaces (automatic detection with 1000BT front interfaces)
- Eight GPIOs (3.3V LVTTL Level). Each input can be individually configured as an interrupt source.
- Sixteen differential pairs (100 ohm impedance) coming from the expansion IO mezzanine (when installed).