TIC-FEP-VPX6a

Virtex®-6 & QorIQ™ 6U VPX Processing Unit
6U OpenVPX Front End Processor

The **TIC-FEP-VPX6a** is a VPX hybrid processing engine combining the latest generation of FPGAs and processors to deliver very high performance levels per watt.

With its QorIQ™ processor for system management and a PCIe Advanced switch for coupling between the processing nodes, the **TIC-FEP-VPX6a** board expands the flexibility of the two Virtex-6 FPGAs and the VPX high bandwidth serial interfaces.

Two FMC mezzanine sites stretch the adaptability of the board to connect ADC, DAC, general I/Os, video, sFPDP or additionnal FPGA FMC modules. With this combination of high performance CPU, dual FPGAs and FMC sites, the **TIC-FEP-VPX6a** provides the ideal platform for radar, sonar, electronic warfare and other demanding digital signal processing applications.

Description

The **TIC-FEP-VPX6a** is controlled by a P2020 processor integrating an e500 v2 Power Architecture core, a DPFPU, an integrated Sec security engine and peripherals, as well as being fully software compatible with existing PowerPC processors.

The QorIQ provides the usual external interfaces (3*Ethernet, 2*Serial and 3*USB ports). An eUSB slot allows connection to an optional storage module.

The PCIe Advanced switch allows coupling between the processor, the fabric links of the VPX backplane and the FPGAs. (Non transparent configuration is possible for VPC fabric link). Other fabric links of the VPX backplane are directly connected to the FPGAs GTX transceivers. In addition, the two FPGAs are directly interconnected via GTX ports – allowing data rate up to 6,5 Gbps (*), LVDS and single-ended signals.

Each Virtex®-6 FPGA on the **TIC-FEP-VPX6a** is associated with two DDR3 memory banks, supporting an 800 MT/s transfer data rate (per bank), and a bank of SRAM DDRII running at 600 MT/s.

Each Virtex®-6 FPGA is interfaced with its own SPI flash (user parameter storage) and through a Spartan®-6 to the Mirror flash (local bit streams storage - up to four bit streams). With its PCIe link, this Spartan®-6 FPGA (control node) can also manage on the fly downloading of the Virtex®-6 bit streams, offering dynamic reconfiguration of the FPGAs. This control node FPGA is also connected to the backplane via two GTP links.

The FMC sites of the **TIC-FEP-VPX6a** are fully compliant with the FPGA Mezzanine Card standard (VITA 57.1), allowing installation of FMC modules provided by Elma, third-party or users. Each FMC can be equipped with an optional I/O connector to route sixteen differential pairs (100 Ohms) from the FMC module directly to the VPX backplane.

Feature Summary

Processor Unit

- Processing Units
  - o One QorIQ processor P2020, 1GHz, e500 v2 core with :
  - o 1 GB of DDR3 with ECC
  - o 256 or 512 MBytes of NOR Flash
  - o Optional NAND Solid-state Disk (eUSB module)
- Two Xilinx Virtex-6 : SX315T (-1 or -2) or SX475T (-1 only) orLX550T, both offering:
  - o Two banks of DDR3 : 40-bit wide, 1.25 GBytes each
  - o One SRAM DDRII : 18-bit wide / 9 MB
  - o One SPI flash (16 MBytes)
- One Spartan®-6 LX-45T (control Node)
  - o One NOR flash (128 MBytes, for bit streams

VPX Interfaces

- Four PCIe x4 port (from PCIe switch)
- GTX ports (1 or 2 * GTX x8 from each FPGAs)
- Two GTP (from Ctrl node FPGA)
- General purpose I/Os
  - o Two 16LVDS (16 from each FPGAs)
  - o Two 16 differential pairs (16 from each FMC I/O connector)
- GPIOs (from ctrl node FPGA)
- Two Ethernet ports (1000BT or 1000BX - from P2020)
- One RS485/RS232 port
- Two USB 2.0 ports
- PIC µ-controller for System Management (per VITA 46.11)

FMC interfaces (for each site, from FPGAs)

- 80 LVDS
- Four reference clocks
- One GTX x4 link

Front panel interfaces

- One USB 2.0, 1 * Ethernet 1000BT and 1 * console port

Accessories

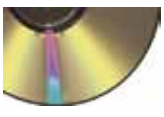
- Engineering kit for debug : JTAG/COP and RS232 console.
- Rear transition module

The **TIC-FEP-VPX6a** is a VPX 6U / 4HP 0.8"(1" on request) board compliant with 6U module definitions of the VITA 46.0 standard. It is available in air cooled and conduction cooled versions compliant with VITA 47 specifications.

ACT/Technico™ brand of Embedded Computing Products

I/O

Design & Documentation



Chassis

Modular Storage

TIC-FEP-VPX6a

Virtex®-6 & QorIQ™ 6U VPX Processing Unit

Our basic firmware manages Freescale's new QorIQ and its internal chipset initialization. This on-board firmware, based on the open-source UBOOT, is an efficient set of software stored in secure flash.

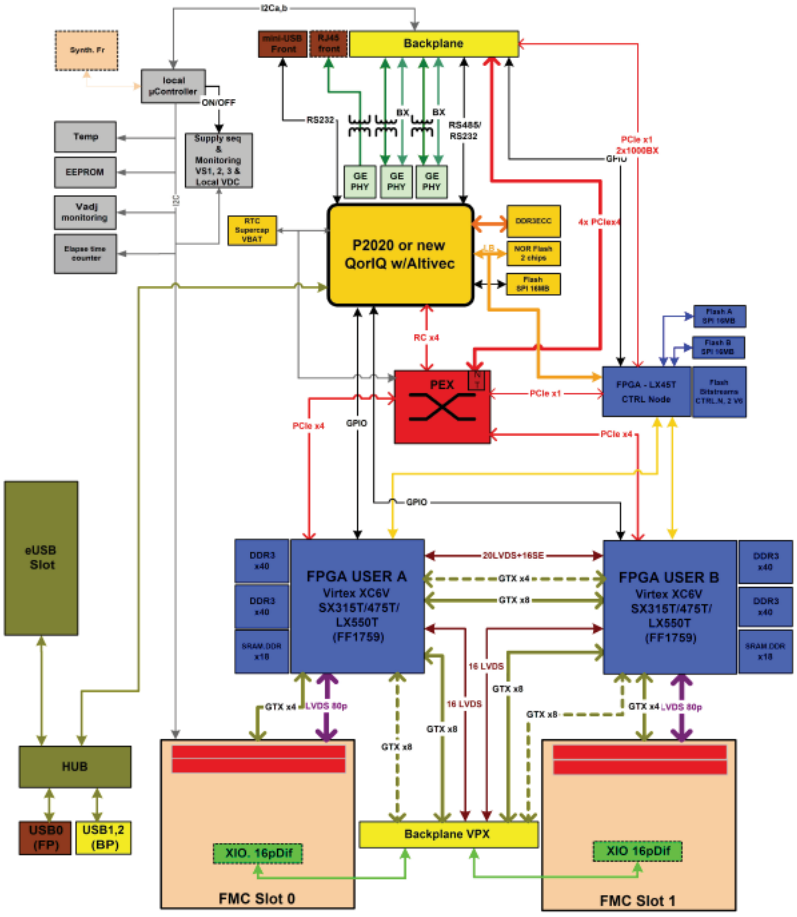
UBoot
Called by the reset vector when the board is powered up, UBoot initializes the processor and performs a set of comprehensive Power-on self-tests (PBIT), before proceeding to different applications determined by the values stored in memory.

IC_Bios
This module allows the user to access the specific TIC-FEP-VPX6a hardware resources via an easy-to-use API. This module is used as a library with Vxworks.

IC-BSP basic
These BSP products are based on the standard distribution of the OS editor. They manage hardware initialization, interrupt handling and generation, hardware clock and timer services, memory management, PCIe management, mapping of memory spaces, serial ports, MAC driver for Gigabit ports and more.

Elma provides BSP for VxWorks® and Linux® operating systems. Other RTOS can be ported on request.

The **TIC-FEP-VPX6a** hardware platform is compatible with the Xilinx development tools (ISE Design Suite, Platform cable).



Environmental Specifications

Visit our website at www.elmasystems.com for the environmental specifications of all of our network switching products.

Ordering Information

Please contact our sales department at (215)-956-1200
or via email at sales@elma.com.

Elma provides :
- VHDL code for system services (DDR3, SRAM DDRII, PCIe, Aurora, IC FMC interfaces). Implementation requires Xilinx ISE Design Tools.
- Host drivers for the CPU (Linux, VxWorks)

Integration from Xilinx System Generator will be available soon.

Users implement their own real-time applications with the capability to integrate the existing open Source code or third-party IP cores.